Patent Claims

1. Method of generating defects in a lattice structure of a semiconductor material during thermal treatment of the material, in which the concentration and/or distribution of defects or vacancies are controlled as a function of a process gas atmosphere.

2. Method according to claim 1, characterized in that the defects are vacancies (empty lattice positions).

3. Method according to claim 1 or 2, characterized in that the defects are semiconductor- substrate atoms on interstitial lattice positions (self-interstitials).

4. Method according to one of the preceding claims, characterized in that the composition of the process gas is controlled.

5. Method according to one of the preceding claims, characterized in that the concentration of the process gas or of the process gas components is controlled.

6. Method according to one of the preceding claims, characterized in that the partial pressure of the process gas is controlled.

7. Method according to one of the preceding claims,

characterized in that the process gas includes a nitrogen-containing gas.

8. Method according to claim 7, characterized in that the process gas includes NH_3.

9. Method according to claim 7 or 8, characterized in that the process gas includes N_2 .

10. Method according one of the preceding claims, characterized in that the process gas contains no oxygen.

11. Method according to one of the claims 1 to 9, characterized in that the process gas includes an oxygen-containing component.

12. Method according to claim 11, characterized in that the oxygen-containing component includes N_2O, No, and/or H_2O.

13. Method according to one of the preceding claims, characterized in that the temperature behavior of the thermal treatment is controlled in terms of time.

14. Method according to one of the preceding claims, characterized in that the process gas atmosphere contains argon.

15. Method according to one of the preceding claims, characterized in that an $Si_xO_yN_z$ layer is produced upon the surface of the semiconductor.

16. Method according to claim 15, characterized in that the thickness of the layer is 0 to 20 angstroms.

17. Method according to one of the preceding claims, characterized in that prior to the thermal treatment a natural SiO_2 layer is removed from the semiconductor surface.

18. Method according to claim 17, characterized in that a Si_3N_4 layer having a thickness of between 0 and 40 angstroms is produced upon the semiconductor.

19. Method according to claim 7, characterized in that the NH_3 concentration is 0 to 10,000ppm.

20. Method according to claim 19, characterized in that the NH_3 concentration is 2500 to 5,000ppm.

21. Method according to one of the preceding claims, characterized in that the thermal stress of the semiconductor wafer is reduced to a minimum.

22. Method according to one of the preceding claims, characterized in that a distribution of foreign atoms within the semiconductor material is controlled via the distribution of the defects.

23. Method according to claim 22, characterized in that the foreign atoms have at least one element of the following group of boron, phosphorus, As, Sb and In.

24. Method according to one of the preceding claims, that the method is carried out on a semiconductor doped with foreign atoms.

25. Method according to one of the claims 1 to 23, characterized in that the method is carried out on a semiconductor that is to be doped.

26. Method according to claim 25, characterized in that the semiconductor is doped.

27. Method according to one of the preceding claims, characterized in that the semiconductor is doped by means of gas phase doping, implantation, and/or diffusion by out-diffusion into the semiconductor from a layer that contacts the semiconductor.

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